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Data driven clock gating technique for dynamic power reduction in digital design

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ABSTRACT

In this paper we demonstrate data driven clock gating technique for power reduction by taking an example of linear feedback shift register (LFSR). We experiment this technique on a 4-bit and 8-bit LFSR designs. Experimental results show that dynamic power can be reduced by a factor of two, for the same functionality of the circuit. The LFSR circuit implemented on a Spartan-6 FPGA platform. Xilinx Power Analyzer tool helps in obtaining the dynamic power analysis of the circuit.

KEY WORDS: Low power, Dynamic power consumption, Data-driven clock gating, Toggling, FPGA implementation.

1. INTRODUCTION

The system clock signal in any digital circuit itself consumes about 70% of total power consumption. In digital circuits clock signal is used for synchronization with inputs and outputs. As clock is applied to every component of the circuit, due to continuous switching of the clock dynamic power is dissipated. Thus the dynamic power dissipation more than half-half of the of total power dissipation in a digital circuit. Clock gating concept mainly describes the gating of the clock at a particular instant of time; so that the switching activity is reduced, thereby dynamic power consumption is reduced. Some of the described methods to decrease dynamic power with grouping of flops in a linear feedback shift register (LFSR).The 32 bit LFSR is divided in to eight groups with four flops each. Each flop's input and output is compared with an Exclusive-or gate. Clock signal is fed with a gated clock. Frank described the clock gating insertion by synopsis power compiler tool. Dushyant (2012) described various clock gating concepts based on latch-based, flip-flop based designs. In latch based clock gating, latch is used control the Enable pin. In negative clock cycle, latch is allowed to reflect the change of Enable. In positive clock cycle, output of latch does not reflect. In flip-flop based clock gating, FF is used as control element. When the negative edge of clock arrives, change of enable will be reflected on FF output. If output of FF is high, clock is applied on sequential circuit. The sleep duration is more in FF based clock gating when compared to Latch based clock gating. Sklavos described the architecture level comparison of two-way shift register in which the existing architecture is differed by adding a control block and with multiplexers. Soma Naidu (2013), described the concept of multi-bit flip flop, the two flip flop can merged in to a single flip flop with a single clock and avoids the duplicating of inverters in the clock path. By doing so clock skew is reduced and small area and delay is found. Chao described three-step LFSR architecture with both higher hardware efficiency and speed. Generator polynomials for the first and third steps are constructed with iterative small length polynomials, which can in turn be easily handled by proposed look-ahead pipelining algorithm. A new scheme is also proposed for cutting down the iteration bound of the LFSR structure in the second step. This architecture can be applied to any LFSR structure for high-speed parallel implementation. Programmable clock gating is a technique used in Soc. In Soc there are many IP cores so in order to reduce the power consumption of the Soc model initially the IP core power should be minimized such that the total power consumption is reduced. In-order to reduce the IP core power a programmable clock gating method is used in this which uses a control register to apply a gated clock to IP core. This control register is configured using user software write. When the users write '0' to control register then the clock is disabled, hence dynamic power consumption is reduced. When the users write '1' to control register the clock is enabled and IP core continues to work. The output of control register is applied to an AND gate with clock hence the output of the AND gate is gated clock. This gated clock is applied to the IP core depending upon the control register. The major drawback of PCG is user to write the enable signal. Such drawback can be overcome by using Adaptive clock gating. The adaptive clock gating technique consisting of finite state machine (FSM) for every IP core with idle, ready, run and with some other states. When particular IP has finished its work then it will be in idle state and there will be no clock applied at this state. The remaining IP remain in working state hence there is a clock applied at this state.

2. EXPEIMENTAL

Data-driven clock gating: When a logic unit is clocked, the sequential elements receive the clock and logic gates inside the sequential circuit switches at every clock edge irrespective of their output changes which leads to huge amount of dynamic power reduction. By clock gating technique, clock is disabled to the unused block, thus avoiding power dissipation due to unnecessary switching of the unused circuit. In clock gating clock is stopped for a portion of circuit which is not performing any active computation. Local clocks that are conditionally enabled are called

gated clocks. In this clock gating technique, the local clock signals are gated using input and output data dependency logic, which called as data driven clock gating technique.

Fig.1 (a) shows a D flip-flop in which the gated clock is applied by Anding with clock signal and enable, thereby reducing switching activity .Hence the dynamic power is reduced. An additional power saving is achieved by a new approach called modified data driven clock gating shown in Fig.1 (b). In this approach the present input is compared with past output by XOR. The obtained XOR output is Anded with clock signal and provided as gated clock to the flip-flop, by doing so the switching activity is reduced and flip-flop toggles only when the past output differs with the present input.

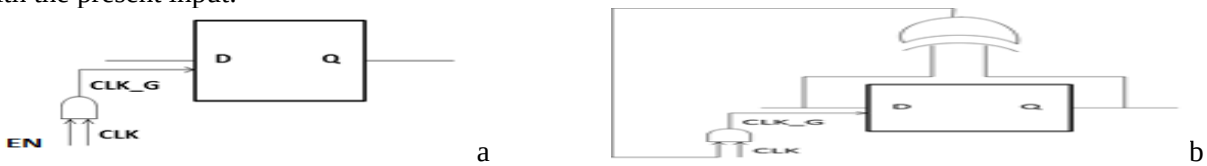

Fig. 1 (a) Clock gating, (b) Modified data-driven clock gating

Linear feedback shift register: A linear feedback shift register is a sequential shift register with combinational logic that causes it to pseudo-randomly cycle through a sequence of binary values. Linear feedback shift register is used in many digital circuits. It is a shift register whose input bit is a linear function of its previous state and is obtained with an array of flip-flops with a linear feedback performed by several XOR gates. They can be efficiently described through an n^{th} order polynomial.

$$P_n(x) = x^n+b_{n-1}x^{n-1}+------+x^1b_1+1$$

Where the binary coefficients b_i, define the well-known polynomial characteristic which the generator main properties depend on. As it is well known, LFSR exhibit a high speed bit generation and they also have good statistical properties. However, the main drawback for these generators is high power consumption. The clock path toggles at every clock cycle, hence dissipating a significant amount of power especially at high clock rate. The power consumption of data path, or gates and gates depends on the switching activity of the inner node. A traditional LFSR with general clock gating approach has one solution to reduce power consumption of LFSR by sending clock to LFSR only when the clock is necessary for LFSR. Basically LFSR's are classified in to two types namely Internal lsfr and External LFSR. The test patterns generated by internal and external LFSR's differ.Fig.2 and Fig.3 shows the structure of external and internal LFSR respectively.

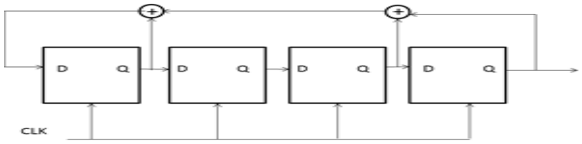

Fig.2. External LFSR

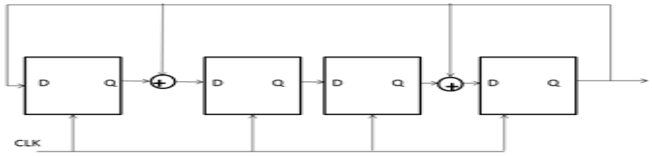

Fig.3. Internal LFSR

4-bit LFSR and 8-bit LFSR without data-driven clock gating: A 4-bit internal LFSR without clock gating is shown in fig 4. It has four D flip flops and an OR gate connected in particular manner.

$P_4(x) = 1+x+x^3$

The above equation defines the 4-bit characteristic polynomial. The equation is represented by observing the feedback path from the flop's to the xor gate. For the above LFSR when we give a test input as '0001', it will generate the sequence as '0010', '0100' …. '1001', '0001' and so on.

An 8-bit external LFSR without clock gating is shown in fig 3. It has eight D flip flops and an OR gates connected in particular manner.

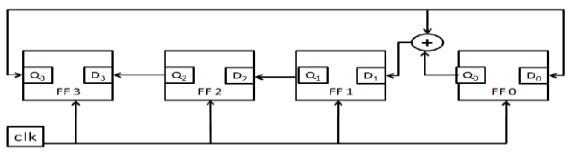

Fig. 4. 4-bit LFSR without data-driven clock gating

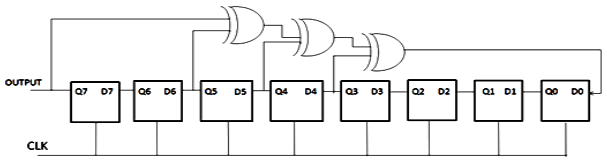

Fig.5. 8-bit LFSR without data-driven clock gating

$P_8(x) = 1+x^3+x^4+x^5+x^7$

The above equation defines the 8-bit characteristic polynomial. The equation is represented by observing the feedback path from the flop's to the xor gate. For the above LFSR when we give a test input as '00000001', it will generate the sequence as '00000010', '00000100', '00001000', '00010001', '00100011…. , '00000001' and so on.

Design and implementation of 4-bit and 8-bit with modified data driven clock gating: The proposed design of 4-bit LFSR and 8-bit LFSR with modified data-driven clock gating is shown in Fig.3 AND Fig.4 respectively. The functionality of 4-bit LFSR circuit is tested with input sequence '0001', it generates the sequence as '0010', 0100'….'1001', '0001'. Similarly the functionality of 8-bit LFSR circuit is tested with input sequence '00000001', it generates the sequence as '00000010', '00000100' 00001000……., '00000001'.Hence the functionality of the

circuit is unaltered. Also, the switching activity is reduced as the gated clock is applied with XORING the present input with past output. Therefore dynamic power of 4-bit LFSR is reduced to a factor of 'x/2' when compared with conventional LFSR. Similarly for 8-bit it is reduced to a factor of 'x/4' than that of circuit without data driven clock gating. Hence when the same technique is applied for larger circuits the dynamic power is dramatically decreased, leads to reduce the overall power consumption.

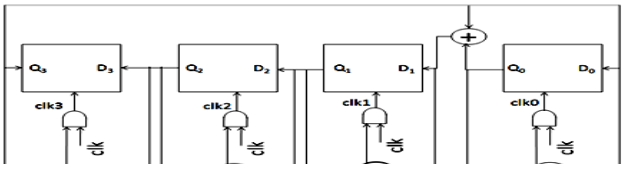

Fig.6. 4-bit LFSR with data-driven clock gating

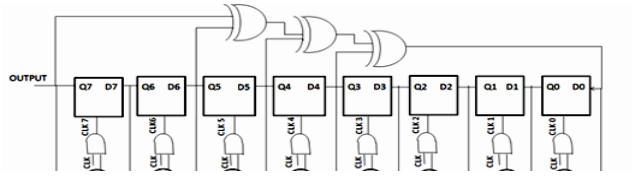

Fig.7. 8-bit LFSR with data-driven clock gating

This circuit has been realized using Verilog language and verified its functionality using XILINX ISE simulator. This data driven clock gated linear feedback shift register implemented on SP605 embedded evaluation kit which has Spartan-6 LX45T FPGA.

Implementation on Spartan-6 FPGA: The FPGA implementation flow showed in Fig 4. Which follows tarting with LFSR specifications, writing Verilog code to realize LFSR with data driven clock gating, verifying functionality using functional verification.

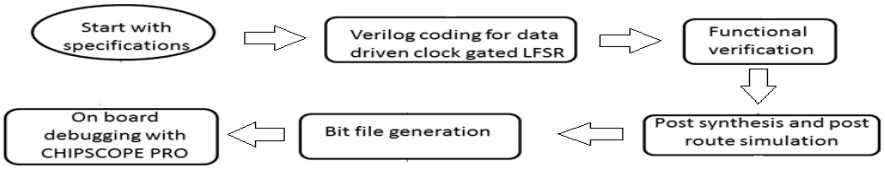

Fig.8.FPGA implementation flow

A bit file has been generated for the data driven clock gated 4 bit linear feedback shift register using Xilinx ISE tool. The functionality of LFSR has verified using CHIPSCOPE PRO debugger tool of Xilinx.

3. RESULTS

The experimental results of a 4-bit LFSR and 8-bit LFSR with and without modified data-driven clock gating simulation results are validated using Xilinx ISE simulator. Simulation results are showed in Fig.5 and Fig.6.

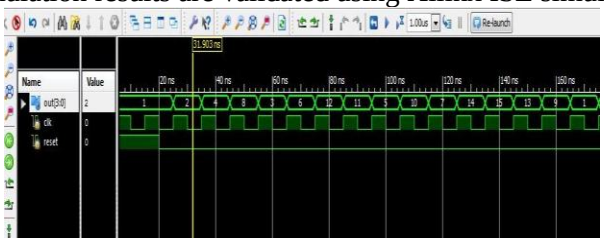

Fig.9.Functional simulation result of 4-bit LFSR

Fig.10.Functional simulation result of 8-bit LFSR

The functional simulation results for both with and without data-driven clock gating observed to be same. And the functionality of liner feedback shift register has verified by post synthesis simulation and post route simulation also.

Power analysis: The power consumption of a 4-bit and 8-bit linear feedback shift registers (LFSR) with and without data-driven clock gating are tabulated in Table 1. Xilinx power analyzer tool is used to get these power results. This Xilinx power analyzer toll takes post placement file (.ncd) of LFSR and constrains as input and generates power results. By observing above power results we can conclude that the dynamic power consumption is reduced by using data driven clock gating concept on LFSR. The power results are verified at a high clock frequency of 1000Mhz.The below figures shows the power analysis results.

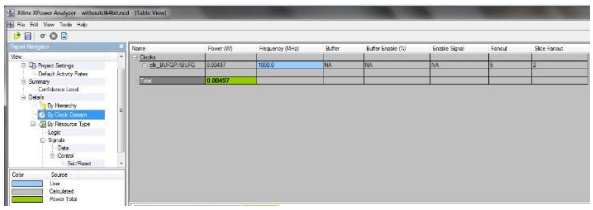

Fig.11.Clock domain for 4-bit LFSR without data driven clock gating

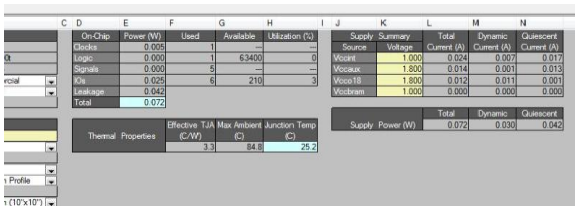

Fig.12.Power analysis for 4-bit LFSR without data driven clock gating

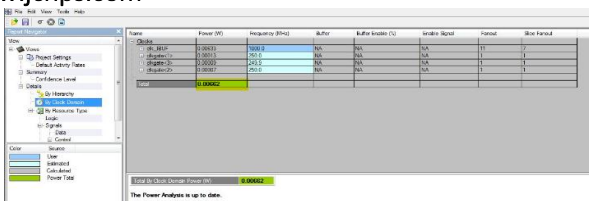

Fig.13.Clock domain for 8-bit LFSR without data driven clock gating

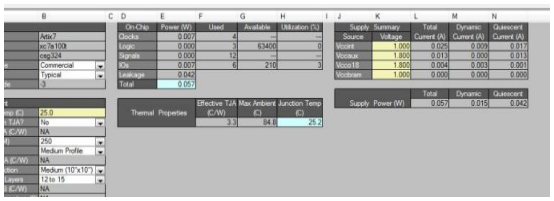

Fig.14.Power analysis for 8-bit with data driven clock gating

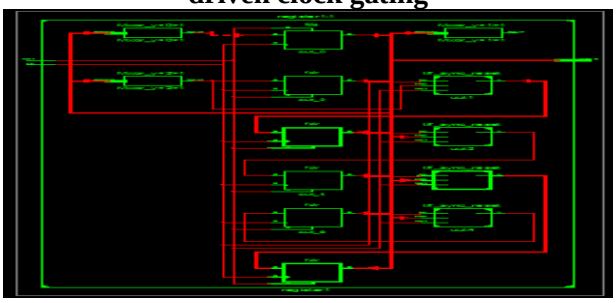

Fig.15.RTL schematic of 4-bit LFSR without clock gating

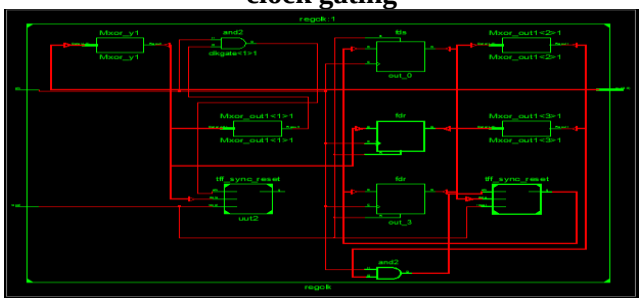

Fig.16.RTL schematic of 4-bit LFSR with clock gating

Table.1.Power consumption results

Design	Power consumption results		
	Total power (w)	Dynamic power(w)	Quiescent power(w)
4-bit LFSR without data-driven clock gating	0.072	0.030	0.042
4-bit LFSR with data-driven clock gating	0.057	0.015	0.042
8-bit LFSR without data-driven clock gating	0.125	0.082	0.043
8-bit LFSR with data-driven clock gating	0.062	0.020	0.042

4. CONCLUSION

The data driven clock gating technique has applied on a 4 bit and 8 bit linear feedback shift register and implemented on FPGA. Power analysis using Xilinx power analyzer tool shows that by using data driven clock gating technique to linear feedback shift register, the dynamic power reduced by half.

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